

**IN THE CLAIMS**

1. (Currently Amended) A method for fabricating a silica microstructure comprising a planar light wave circuit (PLC) havng first and second silica layers, fabrication- method comprising the steps of:

depositing an etch stop layer formed of one of gold, platinum, and alumina on an etching area of a portion of ~~a~~the first silica layer formed on a semiconductor substrate;

forming ~~the~~a second silica layer on the surfaces of the etch stop layer and the first silica layer;

forming a mask patterned according to the shape of the etching area on the surface of the second silica layer;

removing the second silica layer from the etching area using the mask by dry etching according to a predetermined verical profile; and

removing the etch stop layer by wet etching.

2. (Cancelled).

3. (Previously Amended) The silica microstructure fabrication method of claim 1, wherein the etch stop layer deposition step comprises the steps of:

forming the etch stop layer on the first silica layer;

forming a photoresist layer on the etch stop layer;

patterning the photoresist layer according to the shape of the etching area; and

dry-etching the etch stop layer using the photoresist pattern.

4. (Previously Amended) The silica microstructure fabrication method of claim 1, wherein the etch stop layer is formed of one of metal and ceramic.

5. (Previously Amended) The silica microstructure fabrication method of claim 1, wherein the mask formation step comprises the steps of:

forming a metal layer on the second silica layer by sputtering;

forming a photoresist layer on the metal layer;

patterning the photoresist layer according to the shape of the etching area; and

etching the metal layer using the photoresist pattern.

6. (Previously Amended) The silica microstructure fabrication method of claim 1, wherein the first and second silica layers are formed by deposition.

7. (Previously Amended) The silica microstructure fabrication method of claim 1, wherein the second silica layer is dry-etched by RIE (Reactive Ion Etching).

8. (Cancelled).

9. (Cancelled).

10. (Currently Amended) A silica microstructure comprising a planar light wave circuit (PLC) having first and second silica layers which is produced by the steps of:

- depositing an etch stop layer formed of one of gold, platinum, and alumina on an etching area of a portion of the first silica layer formed on a semiconductor substrate;
- forming the second silica layer on the surfaces of the etch stop layer and the first silica layer;
- forming a mask patterned according to the shape of the etching area on the surface of the second silica layer;
- removing the second silica layer from the etching area using the mask by a reactive ion dry etching (RIE); and
- removing the etch stop layer by wet etching.

11. (Cancelled).

12. (Previously Amended) A silica microstructure according Claim 10, wherein the etch stop layer deposition step comprises the steps of:

- forming the etch stop layer on the first silica layer;
- forming a photoresist layer on the etch stop layer;
- patternning the photoresist layer according to the shape of the etching area; and
- dry-etching the etch stop layer using the photoresist pattern.

13. (Previously Amended) A silica microstructure according Claim 10, wherein the etch stop layer is formed of one of metal and ceramic.

14. (Amended) A silica microstructure according Claim 10, wherein the mask formation step comprises the steps of:

forming a metal layer on the second silica layer by sputtering;

forming a photoresist layer on the metal layer;

patterning the photoresist layer according to the shape of the etching area; and

etching the metal layer using the photoresist pattern.

15. (Amended) A silica microstructure according to Claim 10, wherein the first and second silica layers are formed by deposition.

16. (Cancelled).

17. (Amended) A silica microstructure according to Claim 10, wherein the second silica layer is removed according to a predetermined vertical profile.

18. (Cancelled).

19. (Cancelled).

20. (Amended) A silica microstructure according to Claim 17, wherein said microstructure comprises one of a planara lightwave circuit and a microelectromechanical (MEMS) device.

21. (New) A silica microstructure comprising one of a planara lightwave circuit and a micr-electromechnaical system (MEMS) havng first and second silica layers which is produced by the steps of:

depositing an etch stop layer formed of one of gold, platinum, and alumina on an etching area of a portion of the first silica layer formed on a semiconductor substrate;

forming the second silica layer on the surfaces of the etch stop layer and the first silica layer;

forming a mask patterned according to the shape of the etching area on the surface of the second silica layer;

removing the second silica layer from the etching area using the mask by dry etching according to a predetermined vertical profile; and

removing the etch stop layer by wet etching.

22. (New) A silica microstructure according Claim 21, wherein the etch stop layer deposition step comprises the steps of:

forming the etch stop layer on the first silica layer;

forming a photoresist layer on the etch stop layer;

patterning the photoresist layer according to the shape of the etching area; and

dry-etching the etch stop layer using the photoresist pattern.

23. (New) A silica microstructure according Claim 21, wherein the etch stop layer is formed of one of metal and ceramic.

24. (New) A silica microstructure according Claim 21, wherein the mask formation step comprises the steps of:

forming a metal layer on the second silica layer by sputtering;

forming a photoresist layer on the metal layer;

patterning the photoresist layer according to the shape of the etching area; and

etching the metal layer using the photoresist pattern.

25. (New) A silica microstructure according to Claim 21, wherein the first and second silica layers are formed by deposition.

26. (New) A silica microstructure according to Claim 21, wherein the second silica layer is dry-etched by RIE (Reactive Ion Etching).